

REMARKS

Claims 1, 2, and 4-12 are pending in the present application. Claims 1, 9 and 10 are amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached page is captioned “**Version with Markings to Show Changes Made**”.

The specification stands objected to for an informality listed at paragraph 5 of the Office Action. This informality is believed to be cured by the amendment to claims 9 and 10 above. Entry of the amendment and removal of the objection are respectfully requested.

Claims 1-12 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Laparra *et al.* (U.S. 6,319,796 - hereinafter “Laparra”) in view of Park *et al.* (U.S. 6,326,282 - hereinafter “Park”) and Shin *et al.* (U.S. 6,184,077 - hereinafter “Shin”). It is requested that this rejection be reconsidered and removed in view of the foregoing amendment and the following remarks.

The present invention as claimed in amended independent claim 1 is directed to method for providing trench isolation in a semiconductor device. An etching mask pattern is formed on a semiconductor substrate to expose a predetermined region of the semiconductor substrate. The exposed semiconductor substrate is then etched, using the etching mask pattern as an etching mask, to form a trench. An insulating layer is formed over the trench and nearby regions, the insulating layer filling the trench. A high-temperature oxide (HTO) layer is provided on the insulating layer, the HTO layer being formed at a temperature of 700C to 800C. In this manner the underlying insulating layer is densified during formation of the HTO layer. The HTO layer and the insulating layer are planarly etched down to a top surface of the etching mask pattern to form a device isolation layer pattern in the trench. The exposed etching mask pattern is then

removed. (emphasis added)

In this manner, the method of the present invention as claimed in amended claim 1 provides for densification of the insulating layer (see for example, reference 23 of FIG. 1F), during formation of the HTO layer (reference 24 of FIG. 1F) at a temperature of 700C - 800C, Accordingly, there is no need to perform a subsequent, additional annealing process in order to densify the underlying insulating layer, which otherwise could lead to a number of process limitations, as specified in the present application as filed at page 2, lines 2 - 23.

The Office Action states at paragraph 4 that "Laparra and Park disclose all of the steps of claims 1, 2 and 4-12, except for the material layer being formed at a temperature of 500C and higher". In response to this assertion, the Applicants note that claim 1 as amended in Amendment A, filed by the Applicant on July 10, 2002, states that the "HTO layer" is "formed at a temperature of 700C - 800C", and not in the "range of 500C and higher" as originally claimed, and as stated in the Office Action.

Further, the Office Action states at paragraph 4 that "the examiner takes official notice that an LPCVD TEOS film is formed in the temperature range of 500C and higher as can be seen in Shin, column 5, lines 16-18" (emphasis added). While that Applicants agree that Shin discloses this process of forming an LP-TEOS layer at "not less than 650C", at the same time, the Applicants assert that none of the claims of the present invention as amended in Amendment A claim formation of the "material layer" 24 by the LPCVD-TEOS method. Instead, the claims state that the material layer comprises a "high-temperature oxide (HTO) layer", that is "formed at a temperature of 700C-800C". The Applicants note that in the TEOS process, carbon introduced in the source material tetraethosiloxane, $\text{Si}(\text{OC}_2\text{H}_5)_4$ has a high degree of penetration into the active area at the high temperature of "not less than 650C" stated in Shin. Such penetration of carbon into the active area results in degrading of the characteristics of the resulting semiconductor device, as is well known in the art. In view of this, the TEOS process is generally

performed at a low temperature for formation of device isolation structures, and therefore, TEOS is not an acceptable replacement for the HTO process as claimed in the present invention.

None of the references, alone, or in combination, teach or suggest “providing a high-temperature oxide (HTO) layer on the insulating layer” in a trench isolation process. Specifically, Laparra teaches providing a “continued application of a silica-based material” in an “HDP deposition” process to form coating 40b in a preferred embodiment (see Laparra, column 5, lines 6-11). Laparra also suggests application of a low-pressure chemical vapor deposition (LPCVD) of a TEOS-based dielectric, in an alternative embodiment (Laparra, column 5, lines 51-57). At the same time, Park discloses application of a “PE-TEOS or PE-OX layer” as stress-relieving material layer 118. Shin, while mentioning various compositions and application approaches for forming an “etch blocking layer” 127, has nothing to do with trench isolation, and is cited in the Office Action as supporting a temperature range for the LPCVD-TEOS film deposition process.

In addition, none of the references, alone or in combination, teach or suggest densifying “the underlying insulation layer” ... “during formation of the HTO layer” as claimed in amended independent claim 1. Laparra makes no mention of any such densification of the underlying insulation layer 40a at all, let alone during formation of an “HTO layer”, as claimed in amended claim 1. Park, on the other hand, teaches that a subsequent “annealing process is carried out” ... “in order to densify the USG layer” (Park, column 4, lines 66-67). Shin makes no mention of such densification, since Shin is not related to trench isolation. It is therefore submitted that none of the references teach or suggest the combined operation of forming an upper HTO layer, while, during its formation, densifying the underlying insulation layer.

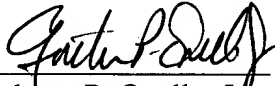
In view of the above, it is submitted that the combination of Laparra, Park, and Shin fails to teach or suggest the present invention as claimed in amended independent claim 1. Accordingly, reconsideration of the rejection and allowance of claim 1 are respectfully requested. With regard to the various dependent claims 2 and 4-12, it follows that these claims should inherit the allowability of the independent claim from which they depend.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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Version with Markings to Show Changes Made

In the Claims:

Claims 1, 9, and 10 are amended above as follows:

1. (Twice amended) A trench isolation method for forming a semiconductor device comprising:

forming an etching mask pattern on a semiconductor substrate to expose a predetermined region of the semiconductor substrate;

etching the exposed semiconductor substrate, using the etching mask pattern as an etching mask, to form a trench;

forming an insulating layer over the trench and nearby regions, the insulating layer filling the trench;

providing a high-temperature oxide (HTO) layer on the insulating layer, the HTO layer being formed at a temperature of 700C - 800C, the insulating layer being densified during formation of the HTO layer;

planarly etching the HTO layer and the insulating layer down to a top surface of the etching mask pattern to form a device isolation layer pattern in the trench; and

removing the exposed etching mask pattern.

9. (Amended) The method of Claim 8, wherein the oxide layer comprises thermal oxide or chemical vapor deposition (CVD) oxide with a thickness of 20Å~200Å [300Å].

10. (Amended) The method of Claim 8, wherein the oxidation barrier layer comprises silicon oxide [nitride] with a thickness of 20Å~300Å.